International Journal of Engineering Science Invention
ISSN (Online): 2319 – 6734, ISSN (Print): 2319 – 6726
www.ijesi.org Volume 2 Issue 6 ǁ June. 2013 ǁ PP.31-35

Parallel Resonance Effect on Conducted Cm Current in Ac/Dc Power Supply

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ABSTRACT: *The paper presents 25A/-48V AC/DC converter finding difficulty of achieving compliance with the conducted emission standard Class A limit (EN55022A), particularly after connecting the output positive line to the earth intended for supplying -48V to telecom system. In order to accomplish this task, different circuit design, components placement and the layout solutions are taken into account to evaluate their effect on the conducted common mode CM noise appeared in AC/DC converter. Likewise, the C_{yL} Y-capacitor input filter choice and placement has been analyzed and assessed. In addition to the circuit composed of the C_Y output Y-capacitor and parasitic inductance of the cable shunting the output positive line to the earth and generating parallel resonance, which, is the source of an excessive conducted CM current at low frequency. This phenomenon meant to be also decisive solution of the generated noise by applying damping technique validated by using simple modeling approach.*

KEYWORDS: *Resonance phenomenon and proposed solutions, modeling and simulation.*

I. INTRODUCTION:

Generally the lack of understanding of EMC fundamentals and switching power supply design rules; relying only on casual placements of devices and components; these are frequently the source of an excessive EMI, which needs hard work to be solved, in addition to the waste of time and money on testing and redesigning the PCB layout.

There are presently many techniques to reduce the EMI emissions of a power converter; some methods include, for example, passive and active filtering, shielding and grounding, noise balancing or cancelling, converter's controls, and packaging design [1, 2-4]. Passive filtering (X-capacitor, Y-capacitors) is the most common method for conducted EMI attenuation. With the inherent functionality of passive components the higher frequency characteristics become less ideal due to the parasitic elements; in fact, it can produce also other noise as *resonance* phenomenon in the conducted noise frequency range. This causes the need for a second filter stage to attenuate the noise at frequencies higher than the bandwidth of the first. A variety of an integrated EMI filters are proposed in [5] for this. However, what can really reduce the cost, and the reproducibility of filter and layout design, it is not only matter of the right choice of the filter, but also the need of analyzing and evaluating the EMI issues before randomly taking any solution process.

In the first part of the paper, the converter structure and its principle operating have been presented, and then conducted EMI measurements have been reported at the converter input with the output filters (X-capacitor and Y-capacitor) before and after connecting the positive line to the earth intended to provide -48V to telecom system.

The conducted EMI standards (EN55022A class A) limit (with average line: violet color) is exceeded at 7.5MHz and at resonance point 1.5MHz. In order to analyze these EMI peaks appeared in the common mode current path and validate the correct choice and placement of C_Y filter. A simple equivalent circuit composed of essential parasitic parameters of the converter, capacitive couplings, inductive couplings, equivalent transient voltage source and the Linear Impedance Stabilization Network (LISN) is evaluated by dimensioning each elements of the whole system including the control circuit loop, and then is used to simulate the resonance influence on common mode current. The simulation results confirm its electrical efficiency.

Finally the combination of all these modifications and resonance damping technique discussed throughout the paper show how the adopted solutions confirmed by the simulation results, allow achieving full compliance of the AC/DC converter conducted emission with the considered standards.

II. MEASUREMENT RESULTS BEFORE APPLIED STRATEGY

2.1 Converter structure and its principle operating

As shown in figure.1 an actual AC/DC converter used for telecom applications, consists of a PFC rectifier circuit with output voltage 400V and switching frequency 50 kHz, followed by a DC/DC converter with

output voltage 48V and switching frequency 140 kHz. Filtering C_y capacitors are connected to the earth. They are used to bypass the CM current I_{cm} flowing into either three input lines.

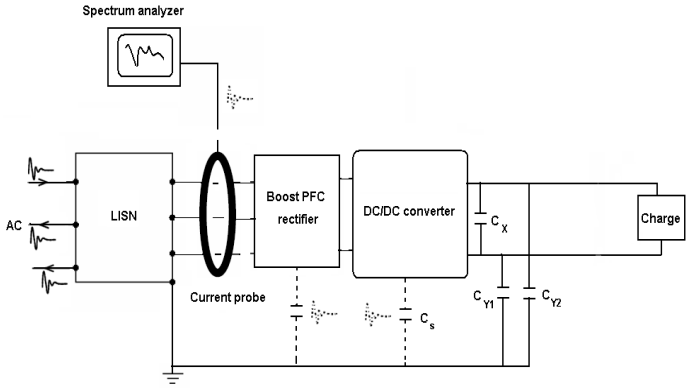


Fig .1 Actual AC/DC converter.

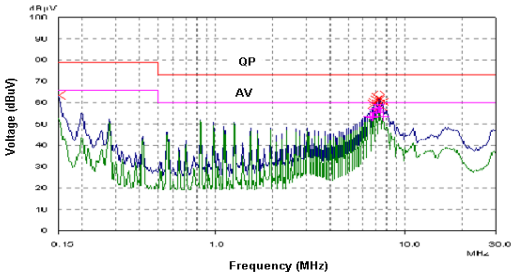
2.2 Test result analysis

The conducted CM current noise measured at the input lines is shown in figure.2. The peak (close to the average limit 60dBuV) created near 7.5 MHz, is due to the capacitive coupling, which leads to increased common mode current picked up by the LISN.

It was hypothesized that the DC/DC stage with high switching frequency would be the origin of the high common mode current measured due to a high dv/dt voltage transitions. Therefore, the voltage source used in the simulated model is the actual transient voltage of the DC/DC converter.

The EMI due to voltage-driven inductive coupling is very likely to exceed the limit at low frequency 1.5 MHz as shown in figure .3. This is occurred after earthing the output-positive cable, which resulted in *parallel resonance* effect on common mode current generated in the victim loop lying just beyond the end of conductive emission limit as illustrated in figure .4. The *parallel resonance* circuit contains two reactive components (cable inductance L_s and C_y), both are influenced by variations in the noise current i_{cm} frequency and both have a frequency point (1.5 MHz) where their two reactive components cancel each other out influencing the characteristics of the circuit. This parallel circuit produces a *parallel resonance* when the resultant current through the parallel combination is in phase with the supply current i_{cm}. At resonance there will be a large circulating current between the inductor and the capacitor due to the energy of the oscillations. This energy is constantly being transferred back and forth between the inductor and the capacitor which results in zero current and great energy being drawn from the supply to the LISN resistance R_{LISN}=50Ω. This is because the corresponding instantaneous values of i_{Ls} and i_{Cy} will always be equal and opposite (180° out of phase) and the total current flowing in a parallel circuit is equal to the vector sum of the individual branch currents and for a given frequency is calculated as: $I_{cm} = I_{RLISN} + I_{Ls} + I_{Cy}$.

The test result versus the frequency is shown in figure .3, where we see that the peak (exceed 60dBuV) value at 1.5MHz is depending on V_{LISN}= 50I_{cm},. Physically, voltage approaches zero at the bottom two sides of the peak in the frequency range because of the short-circuit action by L at low frequencies and by C at high frequencies. In fact, L dominates for f< 1.5MHz, making the parallel circuit inductive, and C dominates for f> 1.5MHz, making it capacitive. In addition, it is readily seen that the noise is maximized toward fundamental and



DC/DC converter switching frequency 140 kHz.

Fig .2 Measured conducted EMI results from the input terminals before earthing the positive line (AV: Average limit- violet line; QP: Quasi peak limit- red line).

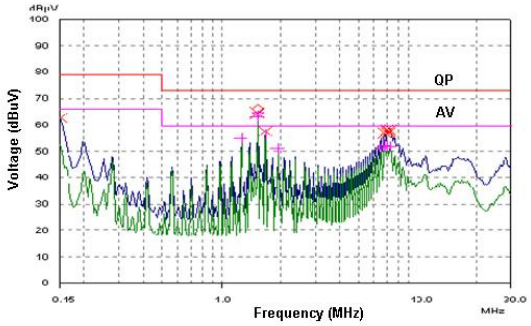


Fig .3 Measured results after earthing the positive line (AV: Average limit- violet line; QP: Quasi peak limit- red line).

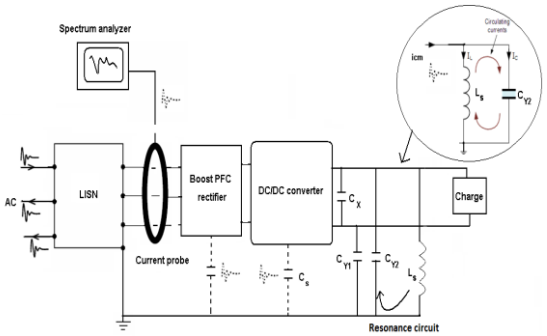


Fig .4 AC/DC converter after connecting the earth to the output-positive cable.

III. MEASUREMENT RESULTS AFTER APPLIED STRATEGY

3.1 Peaks and resonance solutions

a) High frequency peak:

Usually CM current noise depends on proper selection of the filter parameters and their placements in the circuit. The selected circuit model contain: the total series impedance of the stray capacitance, LISN, filter (CM mode choke), and the converter as shown in figure .5. To reduce CM current, it is quite preferable to choose equal values for Y-capacitor C_{yL} and C_{yN} to provide balanced condition between two input lines.

Capacitance below 4.7uF is reasonable value to keep the leakage current below the safety limit. Using these C_Y capacitors, CM current can be suppressed in the higher frequency range to certain limit. However, the results might not be satisfactory because of the by-pass capacitors C_Y are not placed properly in the converter. As shown in figure .5, if common mode choke is inserted in the input circuit, the C_Y must be placed between the CM choke filter and the converter; in order to provide higher impedance of the by-pass capacitor C_Y particularly at high frequency (near 7.5MHz), and then the most of the CM current will flow through C_Y and reduce the noise detected up by the LISN resistance 50Ω to under the average limit (violet line) as shown in figure .6 and figure .7 before and after earthing the positive line. However, by placing C_Y adjacent to LISN at the input lines location, the second resonance can be created, since the impedance of this capacitance is very small at high frequencies and become lower than the LISN impedance 50Ω. Therefore, this prevents the additional common mode current peak caused by the second resonance from flowing through LISN.

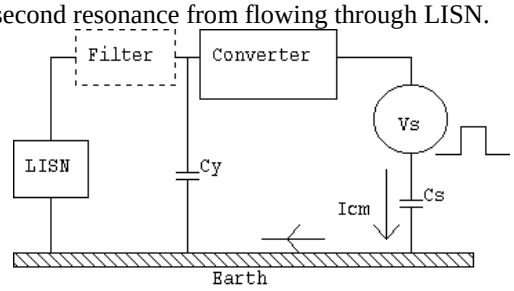


Fig .5 Simplified configuration circuit of conducted common mode current path with inserting C_Y Y-capacitor.

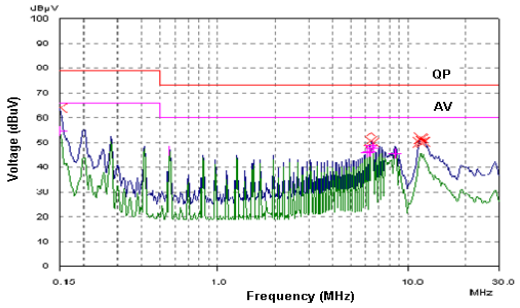


Fig .6 Measured results before earthing the positive line with inserting C_Y=1nF in the input lines.

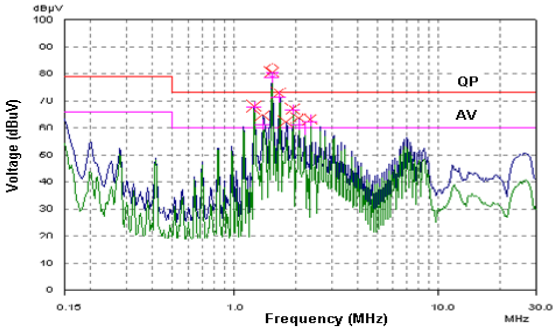


Fig .7 Measured results after
earthing the positive line with inserting C_Y=1nF in the input lines.
(AV: Average limit- violet line; QP: Quasi peak limit- red line).

b) Low frequency peak:

At resonance, the impedance of the parallel circuit is at its maximum value and equal to the resistance of the circuit and we can change the circuit's frequency response by changing the value of this resistance. Changing the value of R_{equ}=R_{LISN}//(R in series with C) affects the amount of current that flows through the circuit at resonance, if both L and C remain constant. Then the impedance of the circuit at resonance Z = R_{equ} is called the "dynamic impedance" of the circuit. Therefore, in order to absorb the conducted CM noise current produced by resonance, a parallel bypassing capacitor C=0.1uF (with low impedance frequencies up to the point of self-resonance) is inserted in series with the damping resistor R=1Ω then shunted with the filtering output Y-capacitor C_Y =1nF, which connects the positive output line to the ground plane as shown in figure .8. Thus, the insertion of such damping filter will reduce the first resonance peak at 1.5 MHz to under average limit as can be seen in figure .9.

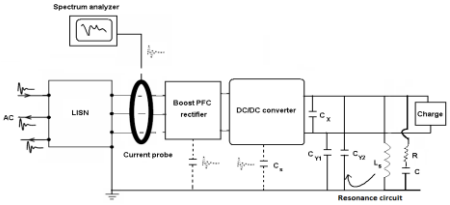
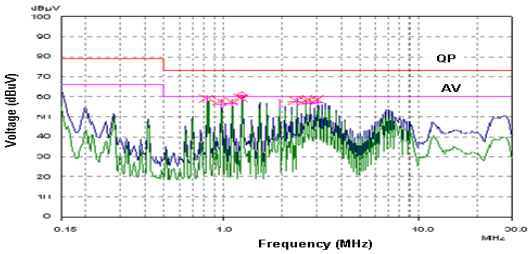


Fig. 8 AC/DC converter with RC damping circuit



. Fig .9 Measured conducted CM EMI results from the input terminals.

After the changes done in the circuit layout and the components parameters, the measured conducted current results shown in the figure .9 seem to be satisfactory and under the specification limit. Therefore, the peak is reduced about 20dB than in the figure .7 and it complies with the conducted emission standard class A limit (EN55022A).

IV. MODEL VALIDATION VERIFIED WITH THE BYPASSING TECHNIQUE

In order to verify the effect of the modification techniques adopted at the AC/DC converter input and the output for parallel resonance solution which lead to CM current reduction, we know that the selected circuit model shown in figure .5 composed of essential CM current circuit branches, and the supply voltage $V_s=V_2$ shown in the figure .10, which is common for all branches, so this can be taken as our reference vector. Each parallel branch must be treated separately so that the total supply current taken by the parallel circuit is the vector addition of the individual branch currents. Then the method available to us is to affect the current in each branch and then add together to obtain i_{cm}. This has been done by adding a damping resistor in parallel with the resonating circuit path which limit it and reduce the total conducted noise currents i_{cm} at 1.5 MHz. The figure .11 shows the CM current simulation result of both resonance peaks appeared at the input lines are less than the average limit 60dBuV, which is matching with the measured conducted EMI result shown in figure .9. The parasitic parameters values used in the model are given by using impedance analyzer HP4194 and commercial software StatMod [6-8].

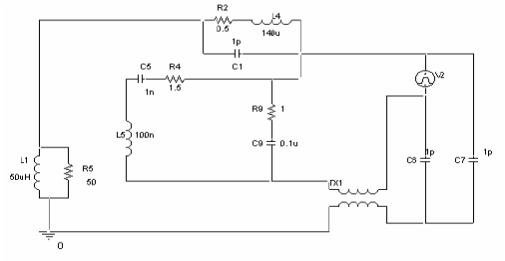


Fig.10 Simulation circuit model.

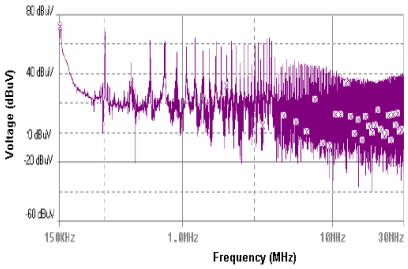


Fig.11 Simulation conducted EMI results.

CONCLUSION

The phenomenon of resonance appears to be a nuisance to be avoided, which affect a variety of applications. In this paper we investigate the parallel resonance circuits appeared in the AC/DC converter, and we characterize its behavior in terms of the frequency response. Next, we examine a resonant circuit consisting of LISN resistance, the output C_{YL} capacitance, and cable inductance. The bypassing technique experimentally tested is used not only for resonance reduction, but also to validate the effectiveness of circuit model based on good understanding of the parasitic elements, the characteristics of components over a frequency range and the PCB interconnections. The matching between the simulation results and the experimental results of the modeling technique confirm the practical solutions adopted for CM current reduction in AC/DC converter.

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